A 16mW, 2.23~2.45GHz Fully Integrated ΣΔ PLL with Novel Prescaler and Loop Filter in 0.35μm CMOS

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Abstract **—A 3mW inherently glitch-free phase-switching prescaler and a loop filter with a 0.2mW capacitance multiplier are proposed for a ΣΔ PLL synthesizer in 0.35μm CMOS. The ΣΔ noise folding is minimized by optimal design of ΣΔ modulator and minimized PLL nonlinearities. The synthesizer has a 9.4% tuning range of 2.23~2.45GHz. The phase noise is –90dBc/Hz at 10kHz, and –128dBc/Hz at 10MHz offset.**

I. Introduction

The ΣΔ-PLL shown in Fig. 1, is a popular fractional-N PLL frequency synthesizer architecture. With a dual-modulus (P or P+1) prescaler and a programmable pulse-swallowing divider (M/A), the nominal divide ratio is

$$N = M \cdot P + A + f \qquad (1)$$

where M and A are programmable integers and f is a programmable fraction.

There are two highlights of the proposed frequency synthesizer, that is, an enhanced low-power and inherently glitch-free phase-switching prescaler, and an area- and power-efficient on-chip loop filter based on a capacitance multiplier [1]. Moreover, the phase noise introduced by the digital ΣΔ modulator (SDM) is minimized by the optimal design of SDM [2], and the reduced nonlinearities of phase-frequency detector (PFD) and charge-pump (CP).

Section II explains the enhanced phase-switching prescaler. The proposed loop filter is covered in section III. Section IV addresses the implementation of other PLL building blocks. Experimental results are presented in section V. Finally, conclusions are drawn in section VI.

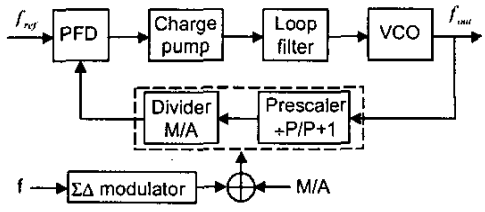

Fig. 1. ΣΔ fractional-N PLL frequency synthesizer

II. Enhanced Phase-Switching Prescaler

The prescaler (PRS) is often the speed bottleneck of PLL synthesizers. The current glitch-removing techniques for phase-switching prescalers [3]-[4] either involve substantial power and/or reduce the operating speed. To overcome this problem, an enhanced inherently glitch-free phase-switching prescaler as shown in Fig. 2 is proposed. One additional divide-by-2 stage is added to further divide down the input signal before phase switching occurs. This stage consists of two master-slave flip-flops (FF's) in parallel to generate eight 45°-spaced phases, $p0$ to $p7$. Since the frequency of input phases is reduced by half (from $f_{in}/4$ to $f_{in}/8$), signal-level amplification is no longer needed and the 8-to-1 MUX can be implemented with standard digital cells to save power. Furthermore, the robustness of the phase switching operation is improved due to relaxed timing requirement.

One problem associated with two divide-by-2 FF's working in parallel is that the eight output waveforms, $p0$ through $p7$, can be either of two patterns. It depends on the initial status of the two FF's and the beginning order of their clock signals. One pattern is that shown in Fig. 3. Compare to this pattern, the phases exchange in signal pairs ($p1$, $p5$) and ($p3$, $p7$) in the other pattern.

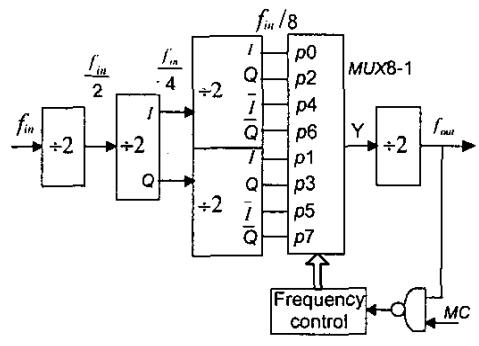

Fig. 2. Proposed enhanced phase-switching prescaler

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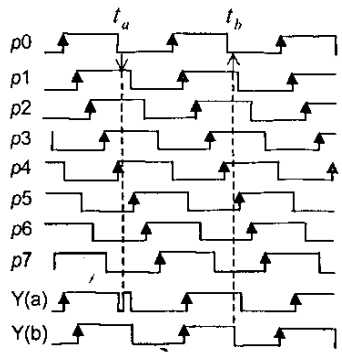

Fig. 3. Inherently glitch-free phase-switching sequence

Fig. 3 illustrates how we change the switching sequence to avoid glitches. The instantaneous divide ratio is increased by 1 when switching occurs in the conventional sequence. As shown in Fig. 3, if the switching from $p0$ to $p1$ occurs at instant t_a where $p0$ and $p1$ have different logic levels, there will be an unwanted glitch at the MUX output $Y(a)$. However, if the switching is reversed from $p1$ to $p0$, that is, the instantaneous divide ratio is decreased by 1, there will be no glitches in the MUX output whenever the switching occurs. The difference can be seen in Fig. 3 where the switching from $p1$ to $p0$ occurs at instant t_b and the MUX output $Y(b)$ is glitch-free although $p0$ and $p1$ have different logic levels at this time instant. Since the proposed architecture is inherently glitch-free, no power-hungry retiming or synchronization circuit is needed for the switching control and the robustness of the switching operation is guaranteed. The division ratio of the prescaler is 15/16. When the mode control (MC) input is high, one switching occurs during the prescaler's output cycle, and the instantaneous divide ratio is 15. Otherwise, no switching occurs and the divide ratio is 16.

To deal with the two possible phase patterns, the phase relationship between $p0$ and $p1$ is detected to self-adjust the switching sequence. If $p0$ leads $p1$ by 45°, the phase switching will occur in the following sequence $p0 \rightarrow p7 \rightarrow p6 \rightarrow \ldots \rightarrow p0$. If $p0$ leads $p1$ by 225°, the switching sequence is $p0 \rightarrow p3 \rightarrow p6 \rightarrow p1 \rightarrow p4 \rightarrow p7 \rightarrow p2 \rightarrow p5 \rightarrow p0$.

III. Loop Filter with Capacitance Multiplier

The loop filter (LF) is a barrier in fully integrating a narrow-band PLL because of its large capacitance. The dual-path topology has been a popular solution to this problem [5]-[6]. Besides increased noise and power due to active devices, the charge-pump of the integration path is still working with a very small current and contributes significant noise. To overcome the constraints of the dual-path topology, a simple capacitance multiplier [7] is used to reduce the capacitance size by a large factor and make it easily integratable within a small area.

A third-order passive loop filter for the charge-pump PLL is shown in Fig. 4. C_1 is the largest capacitor hence it is usually a key integration bottleneck of the PLL.

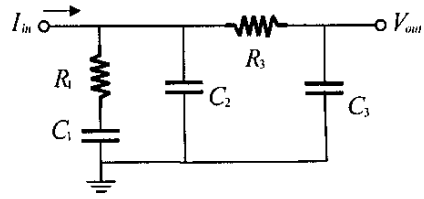

Fig. 4. Third-order loop filter

In this work, the loop filter values are: R_1=10kΩ, C_1=160pF, C_2=10pF, R_3=1kΩ, and C_3=10pF. With PLL loop bandwidth of about 250kHz, the PLL phase margin is about 51°. In TSMC 0.35μm CMOS process, the 160pF poly-to-poly capacitor (C_1) would occupy about 0.2mm^2 of die area. To reduce its area, it was built with a capacitor C_i=160pF scaled up by a factor of 16 as shown in Fig. 5. To minimize the current leakage at node **A**, cascode current mirrors with long-channel transistors are used. The equivalent small signal admittance at the input terminal is:

$$y_{in} = \frac{i_{in}}{v_{in}} = g_{oA} + s\left[C_{p2} + (M+1)C_i \frac{1 + s\dfrac{C_{p1}}{(M+1)g_{m1}}}{1 + s\dfrac{C_i + C_{p1}}{g_{m1}}} \right] \quad (1)$$

C_{p1} and C_{p2} are parasitic capacitors at node **A** and **B**, respectively. Usually, $C_{p1} \ll C_i$ and $C_{p2} \ll C_{p1}$ because C_{p1} includes the large parasitic capacitance between the bottom plate of poly-poly capacitor C_i and ground. g_{m1} is the transconductance of transistor M1, and g_{oA} is the overall conductance at node **A**. M=15 is the current gain of the current mirror (or current amplifier). Fig. 6 shows the simulated frequency responses of y_{in} in comparison with an ideal 160pF capacitor. The three corner frequencies of y_{in} are:

$$\omega_{c1} = \frac{g_{oA}}{C_{p2} + (M+1)C_i} \approx \frac{g_{oA}}{C_1} \quad (2)$$

$$\omega_{c2} = \frac{g_{m1}}{(C_i + C_{p1})} \approx \frac{(M+1)g_{m1}}{C_1} \quad (3)$$

$$\omega_{c3} = \frac{(M+1)g_{m1}}{C_{p1}} \quad (4)$$

ω_{c1} and ω_{c3} are poles while ω_{c2} is a zero. $y_{in} \approx j\omega[C_{p2}+(M+1)C_i] \approx j\omega C_i$ is the intended capacitance in the frequency range of $\omega_{c1} < \omega < \omega_{c2}$.

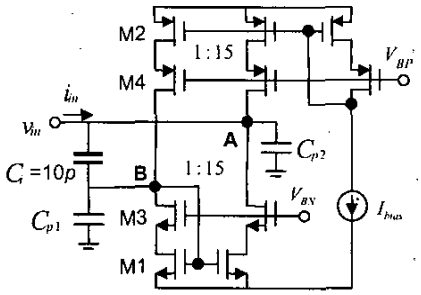

Fig. 5. Loop capacitance multiplier

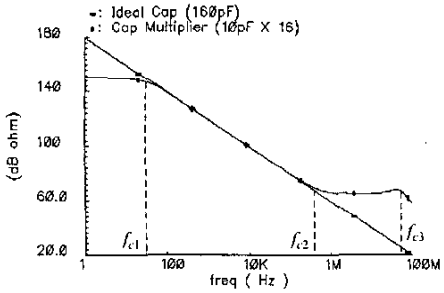

Fig. 6. Simulated impedance of capacitance multiplier

To minimize the current leakage, a small value of g_{oA} is needed to make ω_{c1} as low as possible. Also, the current mismatch between the top and bottom current sources at node **A** must be minimized. Hence we use cascode current mirrors with long-channel transistors.

In the frequency range of $\omega_{c1} < \omega < \omega_{c3}$, (1) yields:

$$y_{in} \approx \frac{s(M+1)C_i}{1+s\frac{C_i}{g_{m1}}} = \frac{1}{\frac{1}{sC_i}+\frac{1}{(M+1)g_{m1}}} \quad (5)$$

Thus in this frequency range, the capacitance multiplier is equivalent to the desired capacitance C_i in series with a resistance of $[(M+1)g_{m1}]^{-1}$ value. We need to reduce the resistance of R_1 by the amount of $[(M+1)g_{m1}]^{-1}$ to keep the zero frequency unchanged. It is obvious that $[(M+1)g_{m1}]^{-1}$ should never be greater than R_1. The simulated resistance at node **A** (=1/ g_{oA}) is around 30MΩ, which is large enough to make the current leakage negligible.

We check the phase noise caused by the capacitance multiplier at 1MHz offset because the phase noise requirement around 1MHz is the most stringent for most of the wireless applications. Since the thermal noise dominates at 1MHz, a simple way is to compare the equivalent noise resistance of the capacitance multiplier with R_1 as far as the noise contribution from R_1 [5] is already negligible. From Fig. 6 we know that the admittance of the capacitance multiplier at 1MHz is approximately $(M+1)g_{m1}$. Neglecting the minimized noise of the bias, the voltage noise density of the capacitance multiplier is approximately given by:

$$v_n^2 = \frac{8kT}{3(M+1)g_{m1}}\left(1+g_{m2}/g_{m1}\right) \quad (6)$$

g_{m2}, which is the transconductance of transistor M2, can be less than g_{m1} for noise optimization. But let us consider the case $g_{m2} \approx g_{m1}$, then the thermal noise of the capacitance multiplier would be less than that of R_1 when

$$g_{m1} \geq \frac{4}{3(M+1)} \cdot \frac{1}{R_1} \quad (7)$$

IV. Other Building Blocks of PLL

Efforts are made in the design of phase-frequency detector (PFD), charge-pump (CP), and digital ΣΔ modulator (SDM), to reduce the PLL nonlinearity and ΣΔ phase noise folding. A PFD similar to the one in [5] is used in this work. The PFD output UP (or DN) is well aligned with its reverse signal $\overline{\text{UP}}$ (or $\overline{\text{DN}}$). A simple charge-pump with fast and symmetry transient response is employed to improve PLL linearity [1].

A third-order three-level SDM as studied in [2] is used to minimize the noise contribution from PFD/CP and ΣΔ phase noise folding. The SDM output is 0, 1, or 2, and it covers the whole fractional range of 0.5 ~ 1.5.

An on-chip LC VCO is designed with spiral inductors. The VCO drives the prescaler directly and no RF buffer or ac coupling is needed. The VCO consumes most of the power because the inductor's Q value is only around 2, and a large output swing is needed to drive the prescaler's pseudo-differential NMOS input pairs.

V. Measurement Results

The chip was fabricated in TSMC 0.35μm CMOS technology through MOSIS. Fig. 7 shows the microphotograph of the whole chip, which includes the monolithic PLL and some standalone blocks for testing. The monolithic PLL has an area of 0.85mm^2 out of which the digital ΣΔ modulator, the VCO, the loop filter and the prescaler occupy 0.5 mm^2, 0.15mm^2, 0.05mm^2 and 0.04mm^2, respectively. The VCO and the prescaler draw 6mA and 2mA from a 1.5-V supply, respectively and other blocks draw 2mA from a 2-V supply in total, whereby the whole PLL system consumes 16mW.

Compared with the 18mW dual-path loop filter in [5], the proposed loop filter with capacitance multiplier only consumes 0.2mW. It is worthwhile to mention that the frequency synthesizer designed in 0.25μm CMOS in [8] failed to work beyond 2.41GHz due to the prescaler of traditional architecture.

Reference spur level is −57dBc with reference frequency of 50MHz. The PLL output tuning range is 9.4%, from 2.23GHz to 2.45GHz. The PLL loop bandwidth is 250kHz. As shown in Fig. 8, the phase noise level at 10MHz offset is −128dBc/Hz, which is mainly limited by the low quality inductor. The spurs caused by the non-ideal 45°-spacing in the phase-switching prescaler are negligible.

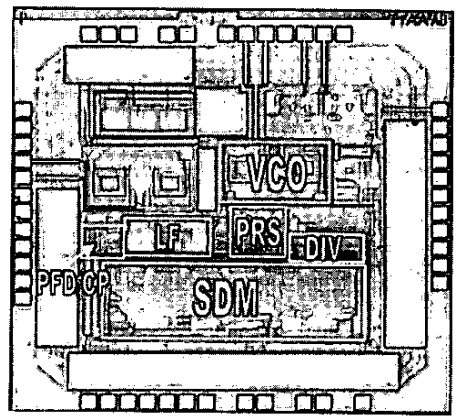

Fig. 7. Chip microphotograph

VI. Conclusion

A monolithic 2.4-GHz ΣΔ fractional-N PLL frequency synthesizer implementation is proposed in 0.35μm CMOS technology. New approaches have been made to tackle the speed bottleneck (the prescaler) and integration bottleneck (the loop filter) of the PLL synthesizer. An enhanced low-power and inherently glitch-free phase-switching prescaler is proposed. Capacitance scaling is deployed to integrate a large capacitor of the loop filter within small die area. Its power and noise are negligible. The PLL operates with 1.5-V (analog), 2-V (digital) and consumes 16mW. Measurement results verified the feasibility and robustness of the enhanced phase-switching prescaler and the practicality of the loop capacitance multiplier.

Note that, the digital SDM takes about 60% of the total active area of this synthesizer because it consists of three 24-bit accumulators with LSB dithering. Its area might be reduced with shorter bit-length and better dithering techniques.

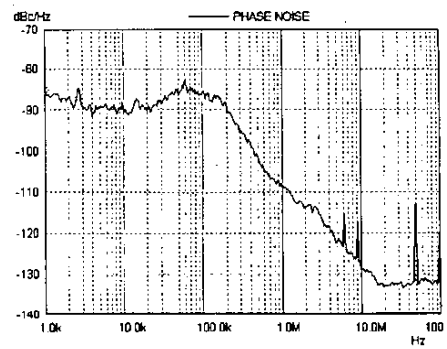

Fig. 8. Measured PLL output phase noise

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